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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,340	KANG ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-45* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *29-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action responds to the Amendment filed 29 March 2004.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 41 and 42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification does not provide support for defining a plurality of integrated circuits across the SOI wafer in the context of the claim. This is new matter.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **29**, 31-38, and new claims 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,251,754 B1 (**Ohshima** et al.) in view of US 5,141,878 (**Benton** et al.) and

Moriceau et al. "Hydrogen annealing treatment used to obtain high quality SOI surfaces" IEEE International SOI Conference, October 1998, pp. 37-38.

Regarding claims 29 and 42, **Ohshima** discloses a method a manufacturing an SOI substrate on which semiconductor devices are to be formed, comprising,

forming a cleaved monocrystalline silicon surface (called "detached surface" at col. 11, lines 36-56) which inherently has some surface roughness;

high temperature annealing the cleaved surface to remove surface roughness (called "flattening the surface") created by the cleaving process (Fig. 3, step P15; Fig. 4D-4E; col. 11, lines 50-56).

Ohshima does not teach the conditions of the anneal.

Benton teaches the benefits of doing a pre-bake anneal of a rough silicon surface in an HCl-H_2 mixture at a temperature of, for example, 1025 °C which is greater than 1000 °C -- as further limited by instant claims 37-- and between 1000 °C and 1200 °C --as further limited by instant claim 45-- to "reduce native oxide films and to further smooth" the silicon wafer, wherein an exemplary anneal mixture is 0.9 liters/min HCl and 40 liters/min H_2 or a ratio of HCl:H_2 of 0.0225, which falls between 0.001 and 30, as further limited by instant claim 32. (See col. 2, lines 45-53.)

It would be obvious for one of ordinary skill in the art, at the time of the invention, to use the roughness-reducing, HCl-H_2 etchant anneal of **Benton** as the high temperature anneal of **Ohshima**, because **Ohshima** desires a native-oxide-removing, surface-flattening anneal to prepare the cleaved silicon surface for growth of an epitaxial layer, and because **Benton** provides the successful anneal conditions to provide such desired results.

Then the only difference is that the degree of surface roughness reduction is not indicated in **Ohshima**.

Moriceau discloses exposing a rough silicon surface to an etchant --which is specifically hydrogen (as further limited in instant claim 21)-- while annealing at a temperature of greater than 1000 °C to reduce the silicon surface roughness from about 50 Å to a less than 1 Å. This equates to a reduction in surface roughness of [(50 Å -1 Å)/50 Å] •100 = 98%, which is greater than 90%, as further limited by instant claim 31. (See whole document -- especially third paragraph and Fig. 1.)

Note also that **Moriceau** also teaches that any native oxide is also removed by this etchant anneal, at the second sentence of the fourth paragraph, which is also a desired result of the **Ohshima** high temperature anneal (col. 11, line 55).

It would be obvious for one of ordinary skill in the art, at the time of the invention, to reduce the surface roughness of **Ohshima** by an amount of at least about 90%, as taught by **Moriceau**, because **Moriceau** teaches such surface reduction enables an especially planar surface for the fabrication of semiconductor devices, which is also the object of **Ohshima**.

Note the high temperature annealing of the cleaved surface in H_2-HCl mixture inherently increases the hydrogen concentration of the cleaved surface because the mechanism by which the surface area is reduced is by etching as explained in Moriceau (4^{th} paragraph on the first page) necessarily requires (1) diffusion of the hydrogen to the cleaved silicon surface --as further limited by **instant claim 44**; (2) reaction of the hydrogen with the silicon surface to form various silicon hydrides, e.g. Si-H (surface bonded), SiH_2 (volatile) and SiH_4 (volatile)--the process by

which the hydrogen concentration of the silicon surface is increased; and (3) desorption of the volatile silicon hydrides. Also, because the number of atoms/volume of a silicon surface is

$$2.33\ g/cm^3 \times 1\ mol/28.0855\ g \times 6.022 \cdot 10^{23}\ atoms/mol = 4.88 \cdot 10^{22}\ atoms/cm^3$$

it is inherent that the concentration of hydrogen is at least equal to the atom density because the hydrogen is reacting at least one hydrogen atom to one silicon atom. Accordingly, the limitation that the hydrogen concentration is 10^{21} to $5 \cdot 10^{22}$ atoms/cm^3 is met --as further required by **instant claim 43**. (See MPEP 2112 regarding inherency.)

Regarding claim 33, as noted above in **Benton**, it is the combination of HCl and H_2 interacting with the rough silicon surface that reduces the surface roughness.

Regarding claims 34 and 38, the epitaxial chamber of **Ohshima** is a thermal processing chamber because the anneal is carried out in this environment of the chamber.

Regarding claim 35, the cleaved surface is provided by controlled cleavage in **Ohshima**. (See at least Figs 2A-2F.)

Regarding claim 36, **Ohshima** discloses that the SOI substrate is formed from a donor silicon wafer.

5. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ohshima** in view of **Benton** and **Moriceau** as applied to claim 29 above, and further in view of the article **Tate** et al., "Defect Reduction of Bonded SOI Wafers by Post Anneal Process" Proceedings of the 1998 IEEE International SOI Conference, Oct. 1998, pp. 141-142.

The prior art of **Ohshima** in view of **Benton** and **Moriceau**, as explained above, discloses each of the claimed features except for indicating the heating ramp rate of 10 °C/second or greater.

Tate teaches a method of reducing surface roughness of cleaved SOI wafers using hydrogen etchant in a rapid thermal annealing using rates far greater than 10 °C/second. (See item entitled "3. H_2 anneal with rapid thermal annealer on Smart Cut SOI.")

It would have been obvious for one of ordinary skill in the art, at the time of the invention to modify **Ohshima** in view of **Benton** and **Moriceau,** to use high ramp rates in order to reduce the time required to smooth the surface and to reduce the thermal budget, because **Moriceau** teaches that high ramp rates should be used, and also because **Tate** specifically teaches that rapid thermal annealing works to reduce surface roughness of cleaved SOI substrates in a hydrogen-containing etchant.

6. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ohshima** in view of **Benton** and **Moriceau** as applied to claim 29 above, and further in view of EP 0 553 852 A2 (**Sato** et al.).

The prior art of **Ohshima** in view of **Benton** and **Moriceau**, as explained above, discloses each of the claimed features except for indicating the pressure of the anneal for reducing the surface roughness of the SOI substrate.

Sato teaches using a hydrogen-containing atmosphere to reduce the surface roughness of a silicon surface by greater than 90% to form a planarized surface, wherein the pressure is, *inter*

alia, atmospheric pressure, i.e. 760 Torr. (See col. 24, lines 34-51; col. 25, lines 15-32, for example.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use 1 atmosphere of pressure during the anneal because **Ohshima**, **Benton,** and **Moriceau**, do not indicate or require any specific pressure and because **Sato** teaches pressures of 1 atmosphere as well as elevated or reduced pressure will also work to reduce the surface roughness by greater than 90% to form a planarized surface.

Moreover, Applicant has provided no evidence to indicate that the pressure during the anneal is critical to the reduction of surface roughness. Rather the instant specification teaches away from any such criticality, stating at p. 15, lines 8-9, "Chamber pressure was generally maintained at about 1 atmosphere, **but can be at others too**." (Emphasis added.)

7. Claims 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ohshima** in view of **Benton** and **Moriceau** as applied to claim 29 above, and further in view of Applicant's admitted prior art (**APA**).

The prior art of **Ohshima** in view of **Benton** and **Moriceau**, as explained above, discloses each of the claimed features except for indicating that the various semiconductor devices forming a circuit include a transistor.

APA teaches that it is known in the art to from transistors on SOI substrates.
It would have been obvious for one of ordinary skill in the art, at the time of the invention to form transistors as at least some of the devices of **Ohshima** as transistors in order to form

circuits having amplifiers and switches, which are notoriously well known in the art, as taught by **APA**.

Response to Arguments

8. Applicant's arguments filed 29 March 2004 have been fully considered but they are not persuasive.

Applicant's arguments regarding the rejection under 35 USC 112(1) are noted, but the language used to clarify the claims does not resolve the issue. As presently written the claims require the integrated circuits to "be defined;" in other words, to exist before the cleaving/annealing process. The instant specification supports forming the integrated circuits only **after** the annealing --not **before** the annealing.

Applicant argues that the applied art does not teach the newly added limitation to claims 29 and 42 of "performing a hydrogen treatment to increase a hydrogen concentration of said cleaved main surface," but the increase in hydrogen concentration is necessarily the result of surface smoothing anneal in the hydrogen-HCl environment, as proven in the Moriceau article. Accordingly, the argument is not persuasive.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
6 April 2004